REMARKS

I. Introduction

Applicants express appreciation for Examiner Tran's courtesy and professionalism in conducting a telephonic interview on January 12, 2005. In response to the Office Action dated September 30, 2004, Applicants have amended claim 6 in the manner discussed during the interview so as to address the pending rejection under 35 U.S.C. § 112, first paragraph and second paragraph. Support for this amendment can be found, for example, in Figs. 1-3 and 11-13, and at page 5, lines 9-27, page 6, lines 2-12, and page 35, line 10 to page 36, line 5 of the specification. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that the pending claim is patentable over the cited prior art references.

II. The Rejection Of Claim 6 Under 35 U.S.C. § 112, First Paragraph

Claim 6 is rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Specifically, the Examiner asserts that the claim limitation "first data line pairs are dedicated for a specific location column sub-block memory cells" introduces new matter.

However, as illustrated in Fig. 2 of Applicants' drawings, each of the data lines DL/XDL is connected to one of the bit line pairs BL/XBL selected by the switches 6, where each of the data lines DL/XDL are dedicated for a predetermined column sub-block (e.g., column "0," column "m" and column "n") of the memory cells (see, also, page 5, lines 9-19 of the specification). Nonetheless, in an effort to advance prosecution and as approved by the Examiner, claim 6 has been

amended to recite "...said first data line pairs are dedicated for a predetermined ~~specific location~~ column sub-block of the memory cells" so as to further clarify the claimed subject matter.

Further, the Examiner asserts that the claim limitation "a plurality of second data line pairs... to select specific row location of sub-block data consisting of crossbar crosspoint" introduces new matter.

However, as disclosed at page 35 line 10 to page 36, line 6 of the specification, each of the processor elements is connected with the data line pairs DB/XDB related to its respective memory cell array, where each memory cell array within the memory is connected with the data line pairs DL/XDL. Because the crossbar switches are formed within the memory or within the processor elements, and the data lines DL/XDL can be used as crossbar wirings (see, e.g., page 20, lines 20-22 of the specification), the data line pairs DB/XDB select a predetermined row (e.g., row "00," row "0m," row "10" and row "1m") of the memory cell array for performing access to data transferred between the memory cell array and the processor. The specification also makes this point clear as set forth, for example, at page 36, lines 13-18 and in Figs. 11-13 of the specification. Nonetheless, as discussed and approved by the Examiner, Applicants have deleted and replaced the foregoing claim language to recite "a plurality of second data line pairs to be connected with one of the first data line pairs via ~~by means of~~ the second gate pairs to select a predetermined ~~specific~~ row ~~location~~ of sub-block data consisting of crossbar crosspoint" in an effort to advance prosecution.

Also, the Examiner asserts that the claim limitation "said first gate pairs and second gate pairs are arranged along the side of sub-block sense amplifier" introduces new matter.

However, as disclosed at page 6, lines 2-12 of the specification, the crossbar switches can be laid out in the area of the bit line side of the memory cell arrays adjacent to the sense amplifier area. Additionally, as readily shown in Fig. 2, the switches 4/6 are arranged adjacent to the sense

amplifiers 5. Nonetheless, Applicants have amended claim 6 to recite "said first gate pairs and said second gate pairs are adjacent to ~~arranged along the side of sub-block~~ said plurality of sense amplifiers ~~amplifier~~."

Accordingly, for all of the foregoing reasons, it is respectfully submitted that the foregoing amendments to claim 6, in conjunction with the foregoing explanation, which identifies the relevant portions of the specification that support the claim limitations questioned in the pending rejection, overcome the pending rejection of Claim 6 under 35 U.S.C. § 112, second paragraph.

III. The Rejection Of Claim 6 Under 35 U.S.C. § 112, Second Paragraph

Claim 6 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. The Examiner asserts that the claim term "said data line pairs" lacks antecedent basis. In response, Applicants have amended claim 6 in the manner suggested by the Examiner. It is respectfully submitted that the foregoing amendment to claim 6 addresses and overcomes this aspect of the rejection.

The Examiner further asserts that the claim phrase "a plurality of first data lines...said plurality of processor elements are laid out thereto" is indefinite. In response, Applicants have deleted the foregoing claim language identified in the rejection as the basis for the indefiniteness rejection, and have further amended claim 6 to recite "a plurality of second data line pairs...and said plurality of processor elements are connected to said plurality of second data line pairs." It is respectfully submitted that claim 6, as amended, is clear and definite, and readily understandable by those of skill in the art when read in light of the specification.

Additionally, the Examiner asserts that the claim phrase "said first gate pairs and second gate pairs are arranged along the side of sub-block of the sense amplifiers" is indefinite, because it is unclear what is meant by this phrase.

However, as illustrated in Fig. 2 of Applicants' drawings, the switches 4 and 6 are arranged along the side of the sense amplifiers 5. Specifically, as set forth at page 6, lines 2-12 of the specification, the crossbar switches can be laid out in the area of the bit line side of the memory cell array adjacent to the sense amplifier area. Hence, it is respectfully submitted that those skilled in the art would clearly understand the rejected claim phrase. Nonetheless, in an effort to advance prosecution, Applicants have amended claim 6 to recite "said first gate pairs and said second gate pairs are arranged adjacent to said plurality of sense amplifiers." As the claim would be readily understandable by one of skill in the art, it is respectfully submitted that the foregoing amendment to claim 6 is in compliance with the requirements of 35 U.S.C. § 112, 2nd paragraph, and overcomes the pending rejection.

IV. The Rejection Of Claim 6 Under 35 U.S.C. § 102

Claim 6 stands rejected under 35 U.S.C. § 102(a) as being anticipated by EP 0935252 to Ohtani. Applicants respectfully request reconsideration of this rejection for at least the following reasons.

Claim 6 recites in-part a semiconductor memory comprising a plurality of first data line pairs that are dedicated for a predetermined column sub-block of the memory cells, and a plurality of second data line pairs to be connected with one of the first data line pairs via the second gate pairs to select a predetermined row of sub-block data, wherein the plurality of processor elements are connected to the plurality of second data line pairs.

In accordance with one exemplary embodiment of the present invention, each of the data line pairs DB/XDB is connected with one of the data line pairs DL/XDL, wherein the processor elements 9 are connected to the plurality of data line pairs DB/XDB. As a result, the present invention advantageously provides a memory-embedded processor having a high speed and low power crossbar system formed on a single chip, wherein the system is capable of making plurality of accesses to the plurality of memory cell arrays simultaneously (see, e.g., page 7, line 22 to page 8, line 10 of the specification).

Turning to the cited prior art, at a minimum, Ohtani is silent with regard to providing the local IO line pairs LIO that are dedicated for a predetermined **column** sub-block of the memory cells, or providing the global IO line pairs GIO for selecting a predetermined **row** of sub-block data consisting of crossbar point. Indeed, contrary to the conclusion set forth in the Office Action, Ohtani discloses that the subarray blocks SBAj0 to SBAj7 are each provided with four global IO lines GIOa-GIOd extending in the **column** direction, rather than in the row direction, (see, Fig. 3 and [0019]), while the subarray blocks SBA0i to SBAi7 are each provided with four local IO lines LIOa-LIOd extending in the **row** direction, rather than in the column direction (see, Fig .2 and [0017]).

Even assuming *arguendo* that the local IO lines LIOa-LIOd and the global IO lines GIOa-GIOd of Ohtani correspond to the claimed second data line pairs and first data line pairs, rather than to the respective claimed first data line pairs and second data line pairs as alleged in the Office Action, the memory integrated circuit device of Ohtani only discloses that the local IO lines LIOa-LIOd are connected to the bit lines BL0-BL3 via the column select gate TG1-TG4 and sense amplifiers SA, and does not disclose or suggest that the global IO lines GIOa-GIOd are connected

to the bit lines BL0-BL3 via the column select gate TG1-TG4 and the sense amplifiers SA (see, Fig. 4).

Furthermore, it would appear that Ohtani only discloses that the global IO lines GIOa-GIOd are coupled to the registers and the alleged processors via the registers, and does not disclose or suggest that the alleged processors are connected to the global IO lines GIOa-GIOd.

Thus, for at least these reasons, Ohtani does not disclose or suggest a semiconductor memory comprising a plurality of first data line pairs that are dedicated for a predetermined column sub-block of the memory cells, a plurality of second data line pairs to be connected with one of the first data line pairs via the second gate pairs for selecting a predetermined row of sub-block data, wherein the plurality of processor elements are connected to the plurality of second data line pairs, as recited by claim 6.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)*, and at a minimum, Ohtani fails to disclose or suggest the foregoing claim elements, it is clear that Ohtani does not anticipate claim 6.

Hence, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including

extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: January 28, 2005